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TITLE

DEVICES WITHOUT CURRENT CROWDING EFFECT AT THE FINGER'S
ENDS

5 **BACKGROUND OF THE INVENTION**

Field of the Invention:

The present invention relates to an ESD protection
device and particularly to an ESD protection device
eliminating ESD current crowding events, so that a higher
10 ESD level may be achieved under MM ESD testing.

Description of the Prior Art:

ESD damage has become one of the main reliability
concerns facing IC (integrated circuit) products.
15 Particularly, when scaled down to the deep sub-micron regime
and the thinner gate oxide, the MOS become more vulnerable
to ESD stress. For general industrial specifications, the
input and output pins of IC products must sustain HBM
(Human-Body-Model) ESD stress of over 2000V and MM (Machine-

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Model) ESD stress of over 200V. Therefore, ESD protection circuits must be placed around the input and output (I/O) pads of the IC to protect IC against the ESD stress.

ESD protection devices are frequently drawn with large
5 device dimensions and realized by finger-type layout to save total layout area. The layout top views and cross-sectional views of the prior arts to improve the ESD level of ESD protection devices by layout method are shown in FIG. 1A and 1B. It is formed on a P silicon substrate 11 and includes a
10 STI (shallow trench isolation) 13 enclosing an active region 12, a P guard ring 14 enclosing the STI 13, two gates 15, each composed of polysilicon layer 151, gate oxide 152 and spacers 153, and N drain and source region 161 and 162 placed in between and on the outer sides of the gates 15.
15 The gates, source region, and body are typically connected to the ground while the drain region is connected to the input/output pad. The fundamental theorem of ESD protection design is based on the mechanisms of the MOS and the parasitic lateral n-p-n bipolar (BJT) under high current,

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and high field conduction. FIG. 2A and 2B are sectional views and an equivalent circuit of a NMOS transistor, with the drain 22 as the collector, substrate 21 as the body and source 23 as the emitter. During ESD stress, high field at the drain causes the N+ to P substrate junction to enter an avalanche breakdown condition, generating excessive electron-hole pairs. The current of the electron-hole pairs forward biases the substrate-source (PN junction), and the voltage drop across the substrate resistances increase the BE junction voltage of the parasitic BJT which is triggered to generate the snapback region in its I-V curves, as shown in FIG. 3. Thus, the parasitic BJT turns on to and bypass the ESD current.

FIG. 4A and 4B are top and sectional views of another conventional ESD protection device, a gate grounded NMOS. With comparison to the ESD protection device in FIG. 1A and 1B, it is noted that the bulk substrate resistance of the BB' region is much larger than that of the AA' region. This allows the parasitic BJT of the BB' region to turn on faster

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than that of the AA' region with higher collector current to
bypass the ESD current and spread through the BB' region.
The parasitic BJT of the BB' region can provide larger
effective area than the AA' region to discharge the ESD
5 current, therefore it may have a high HBM ESD robustness.
However, under MM ESD zapping, the drain node conductivity
with higher peak currents of 3~4 Amps (for 200V MM ESD
stress) often cause ESD damage at the corner or finger's end
regions. The cause of damage is MM ESD current 3 or 4 times
10 higher through an extremely small resistance than the HBM
ESD current. Although the resistance of the AA' region is
smaller than that of the BB' region, the breakdown current
(due to ESD zapping at the drain) of the drain to substrate
junction at the AA' region is still high enough to forward
15 bias and to turn on the parasitic BJT at the AA' region,
before turning on the parasitic BJT at the BB' region.
Thus, an excess of current crowds around the AA' region and
causes device failure at this region. Such damage is

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commonly shown in photographic training materials used in ESD protection design training courses.

SUMMARY OF THE INVENTION

5 The object of the present invention is to provide an ESD protection device eliminating ESD current crowding events to achieve a higher ESD level under MM ESD testing.

 The present invention provides a first ESD protection device comprising a substrate, an isolation region on the
10 substrate, enclosing an active region, a first gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to a first node, a second gate disposed on a first side of the first gate and near the first end of the first gate, and a first and second
15 doping region on the first and a second side of the first gate, and coupled to a second and the first node respectively, wherein the first doping region has a first gap under the second gate.

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The present invention provides a second ESD protection device comprising a substrate, an isolation region on the substrate, enclosing an active region, a first gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to a first node, 5 a second gate disposed on a second side of the first gate and near the first end of the first gate, and a first and second doping region on a first and the second side of the first gate, and coupled to a second and the first node 10 respectively, wherein the second doping region has a first gap under the second gate.

The present invention provides a third ESD protection device comprising a substrate, an isolation region on the substrate, enclosing an active region, a first gate having a first and second end overlapping the isolation region to 15 stretch over the active region, and coupled to a first node, and a first and second doping region on the first and a second side of the first gate, and coupled to a second and

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the first node respectively, wherein the first doping region has a first gap near the first end of the first gate.

The present invention provides a fourth ESD protection device comprising a substrate, an isolation region on the substrate, enclosing an active region, a first gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to a first node, and a first and second doping region on the first and a second side of the first gate, and coupled to a second and the first node respectively, wherein the second doping region has a first gap near the first end of the first gate.

The present invention provides a fifth ESD protection device comprising a substrate, an isolation region on the substrate, enclosing an active region, a first gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to a first node, and a first and second doping region on the first and a second side of the first gate, and coupled to a second and the first node respectively, wherein the isolation region

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protruding into the first doping region near the first end of the first gate.

The present invention provides a sixth ESD protection device comprising a substrate, an isolation region on the substrate, enclosing an active region, a first gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to a first node, and a first and second doping region on the first and a second side of the first gate, and coupled to a second and the first node respectively, wherein the isolation region protruding into the second doping region near the first end of the first gate.

The present invention provides a seventh ESD protection device comprising a substrate, an isolation region on the substrate, enclosing an active region, a first gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to a first node, and a first and second doping region on the first and a second side of the first gate, and coupled to a second and

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the first node respectively, wherein the isolation region has a first portion under the first end of the first gate protruding into both the first and second doping region.

5 The present invention provides an eighth ESD protection device comprising a substrate, an isolation region on the substrate, enclosing an active region, a first gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to a first node, a first and second doping region on the first and a second
10 side of the first gate, and coupled to a second and the first node respectively, and a third doping region disposed under the first and second doping region and near the first end of the first gate, having a doping concentration lower than that of the first and second doping region.

15 The present invention provides a ninth ESD protection device comprising a substrate, an isolation region on the substrate, enclosing an active region, a first gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to a first node,

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a first and second doping region on the first and a second side of the first gate, and coupled to a second and the first node respectively, and a first well disposed under the first doping region and near the first end of the first
5 gate.

The present invention provides a tenth ESD protection device comprising a substrate, an isolation region on the substrate, enclosing an active region, a first gate having a first and second end overlapping the isolation region to
10 stretch over the active region, and coupled to a first node, and a first and second doping region on the first and a second side of the first gate, and coupled to a second and the first node respectively, and wherein the first gate protruding into the first doping region so that, in the
15 first doping region, a width of a center portion is larger than those of portions near the first and second end of the first gate.

BRIEF DESCRIPTION OF THE DRAWINGS

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The present invention will become more fully understood from the detailed description given hereinbelow and the accompanying drawings, given by way of illustration only and thus not intended to be limitative of the present invention.

5 FIG. 1A and 1B are top and sectional views of a conventional ESD protection device.

FIG. 2A and 2B are sectional views and an equivalent circuit of a NMOS transistor.

10 FIG. 3 is a diagram showing a relation between the current and breakdown voltage of a NMOS transistor.

FIG. 4A and 4B are top and sectional views of another conventional ESD protection device.

15 FIG. 5A and 5B are top and sectional views along a line AA' of an ESD protection device according to a first embodiment of the invention.

FIG. 6A and 6B are top and sectional views along a line AA' of an ESD protection device according to a second embodiment of the invention.

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FIG. 7A and 7B are top and sectional views along a line AA' of an ESD protection device according to a third embodiment of the invention.

5 FIG. 8A and 8B are top and sectional views along a line AA' of an ESD protection device according to a fourth embodiment of the invention.

FIG. 9A and 9B are top and sectional views along a line AA' of an ESD protection device according to a fifth embodiment of the invention.

10 FIG. 10A and 10B are top and sectional views along a line AA' of an ESD protection device according to a sixth embodiment of the invention.

FIG. 11A and 11B are top and sectional views along a line AA' of an ESD protection device according to a seventh
15 embodiment of the invention.

FIG. 12A and 12B are top and sectional views along a line AA' of an ESD protection device according to an eighth embodiment of the invention.

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FIG. 13A and 13B are top and sectional views along a line AA' of an ESD protection device according to a ninth embodiment of the invention.

FIG. 14A and 14B are top and sectional views along a line AA' of an ESD protection device according to a tenth embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

First Embodiment

FIG. 5A and 5B are top and sectional views along a line AA' of an ESD protection device according to a first embodiment of the invention. It includes a P silicon substrate 51, STI (shallow trench isolation) 52, a P guard ring 50 enclosing the STI 52, first gates 531 and fourth gate 532, ~~dummy~~ second gates 541-544, third gate 542, fifth gate 543, sixth gate 544 and N drain and source region 551 and 552. The STI 52 is on the substrate 51 and encloses an active region 56. The first gates 531 and fourth gate 532 have two ends overlapping the STI 52 to stretch over the

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active region 56, and are coupled to ground or a pre-driver.

The dummysecond gates 541-544, third gate 542, fifth gate 543

and sixth gate 544 are disposed on a common side and near

each end of the first gates 531 and fourth gate 532. Each

5 of the dummysecond gates 541-544, third gate 542, fifth gate

543 and sixth gate 544 has one end overlapping the STI 52.

The first doping(drain) region 551 and second/third

doping(source) region 551 and 552 are disposed in between

and on outer sides of the first gates 531 and fourth gate

10 532, and coupled to a pad and groundsecond node 556 and

first node 555, respectively. More specifically, the first

node 555 is ground while the second node 556 is a pad. The

first doping(drain) region 551 has first gaps 571-574, second

gap 572, third gap 573, and fourth gap 574, which are

15 undoped, in the substrate under the dummy second gates

541-544, third gate 542, fifth gate 543 and sixth gate 544,

respectively. The gaps 571-574 are formed because the gates

541-544 prevent the substrate under the gates 541-544 from

being doped during source/drain formation. Each of the

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first gates 531 and, fourth gate 532, and dummysecond gates
541-544, third gate 542, fifth gate 543 and sixth gate 544
includes a conducting layer 581 made of polysilicon, an
oxide layer 582 made of silicon oxide under the conducting
5 layer 581 and spacers 583 made of silicon oxide adjacent to
the conducting layer 581 and oxide layer 582.

In the first embodiment, the base width of the
parasitic BJT is directly related to the gate length of the
NMOS and the longer channel transistor will have a lower
10 turned-on efficiency because of lower bipolar efficiency.
The ~~dummysecond gates 541-544,~~ third gate 542, fifth gate 543
and sixth gate 544 at the AA' region are used to increase
the base width of the parasitic BJT at the AA' region and
decrease its turned-on efficiency. While the base width of
15 the parasitic BJT at the BB' region is shorter than it is at
the AA' region, the turned-on efficiency of the BB' region
can be successfully balanced. Therefore, the parasitic BJT
at the BB' region will turn on sooner than it will at the
AA' region, providing a larger bypass ESD current area than

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the AA' region and increasing the high MM ESD level. On the other hand, the HBM ESD level will not decrease while ~~dummy~~second gates 541-544, third gate 542, fifth gate 543 and sixth gate 544 are inserted into the active region 56 under
5 HBM ESD zapping because the bypass ESD current area is almost the same as the devices of the prior arts.

Second Embodiment

FIG. 6A and 6B are top and sectional views along a line AA' of an ESD protection device according to a second
10 embodiment of the invention. With comparison to the ESD protection device shown in FIG. 5A and 5B, it is noted that the ~~dummy~~second gates 541-544, third gate 542, fifth gate 543 and sixth gate 544 are disposed on the source region 552 so that the first gaps 571-574, second gap 572, third gap
15 573, and fourth gap 574 are located in the source region 552 in the ESD protection device of FIG. 6A and 6B. The ESD protection devices in FIG. 5A and 5B, and 6A and 6B have equal ESD performance.

Third Embodiment

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FIG. 7A and 7B are top and sectional views along a line AA' of an ESD protection device according to a third embodiment of the invention. It includes a P silicon substrate 71, STI (shallow trench isolation) 72, a P guard ring 70 enclosing the STI 72, first gates 731 and second gate 732, and N drain 751 and source region ~~751~~ and 752. The STI 72 is on the substrate 71 and encloses an active region 76. The first gates 731 and second gate 732 have two ends overlapping the STI 72 to stretch over the active region 76, and are coupled to ground or a pre-driver. The first doping(drain) region 751 and second/third doping(source) region ~~751~~ and 752 are disposed in between and on outer sides of the first gates 731 and second gate 732, and coupled to a ~~pad and ground~~second node 756 and first node 755, respectively. More specifically, the first node 755 is ground while the second node 756 is a pad. The first doping(drain) region 751 has first gaps 741-774, second gap 742, third gap 743, and fourth gap 744 near each end of the first gates 731 and second gate 732. The first gaps

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~~741-774~~, second gap 742, third gap 743, and fourth gap 744
are formed by an implantation step compatible with a CMOS
process, during which a mask blocks the first gaps
~~771-774~~, second gap 742, third gap 743, and fourth gap 744

5 from N+ ions. Each of the first gates 731 and second gate
732 includes a conducting layer 781 made of polysilicon, an
oxide layer 782 made of silicon oxide under the conducting
layer 781 and spacers 783 made of silicon oxide adjacent to
the conducting layer 781 and oxide layer 782.

10 The layout method of the third embodiment, increases
the AA' region resistance and decreases parasitic BJT
turning on efficiency, making it possible for ESD current to
go through the BB' region under MM ESD zapping. Thus, the
MM ESD current bypasses bigger areas and has a higher MM ESD
15 level than the device structures of prior arts. On the
other hand, the HBM ESD level will not decrease as it ~~will~~
without N+ diffusion between the gates and drain contact at
the AA' region. Moreover, the proposed layout method can

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also be applied to the PMOS to improve its MM ESD robustness.

Fourth Embodiment

FIG. 8A and 8B are top and sectional views along a line
5 AA' of an ESD protection device according to a fourth
embodiment of the invention. With comparison to the ESD
protection device shown in FIG. 7A and 7B, it is noted that
the first gates 741-744, second gap 742, third gap 743, and
fourth gap 744 are located in the second doping(source)
10 region 752. The ESD protection devices in FIG. 7A and 7B,
and 8A and 8B have equal ESD performance.

Fifth Embodiment

FIG. 9A and 9B are top and sectional views along a line
AA' of an ESD protection device according to a fifth
15 embodiment of the invention. It includes a P silicon
substrate 91, STI (shallow trench isolation) 92, a P guard
ring 90 enclosing the STI 92, first gates 931 and second
gate 932, and N type first doping(drain) region 951 and
second doping(source) region 951 and 952. The STI 92 is on

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the substrate 91 and encloses an active region 96. The
first gates 931 and second gate 932 have two ends
overlapping the STI 92 to stretch over the active region 96,
and are coupled to ground or a pre-driver. The first
5 doping(drain) region 951 and second/third doping(source)
region 951 and 952 are disposed in between and on outer
sides of the first gates 931 and second gate 932, and
coupled to a ~~pad and ground~~second node 956 and first node
955, respectively. More specifically, the first node 955 is
10 ground while the second node 956 is a pad. The isolation
regions(STI regions) 941~944 protrudes into the first
doping(drain) region 951 near each first and second end of
the first gates 931 and second gate 932. Each of the first
gates 931 and second gate 932 includes a conducting layer
15 981 made of polysilicon, an oxide layer 982 made of silicon
oxide under the conducting layer 981 and spacers 983 made of
silicon oxide adjacent to the conducting layer 981 and oxide
layer 982.

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The layout method of the fifth embodiment, increases the AA' region resistances and decreases parasitic BJT turning on efficiency, making it possible for ESD current to go through the BB' region under MM ESD zapping. Thus, the MM ESD current bypasses bigger areas and has a higher MM ESD level than the device structures of prior arts. Conversely, the HBM ESD level will not decrease as STI is inserted between the gate and drain contact ~~or below the gate~~ at the AA' region. Moreover, the proposed layout method can also be applied to the PMOS to improve ESD robustness.

Sixth Embodiment

FIG. 10A and 10B are top and sectional views along a line AA' of an ESD protection device according to a sixth embodiment of the invention. With comparison to the ESD protection device shown in FIG. 9A and 9B, it is noted that the STI 941~944 protrudes into the second/third doping(source) region 952. The ESD protection devices in FIG. 9A and 9B, and 10A and 10B have equal ESD performance.

Seventh Embodiment

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FIG. 11A and 11B are top and sectional views along a line AA' of an ESD protection device according to a seventh embodiment of the invention. For the sake of clarity, the same elements in FIG. 11A and 11B, and 9A and 9B refer to the same symbols. The ESD protection device includes a P silicon substrate 91, STI (shallow trench isolation) 92, a P guard ring 90 enclosing the STI 92, first gates 931 and second gate 932, and N type first doping(drain) region 951 and second doping(source) region ~~951~~ and 952. The STI 92 is on the substrate 91 and encloses an active region 96. The gates 931 and 932 have two ends overlapping the STI 92 to stretch over the active region 96, and are coupled to ground or a pre-driver. The first doping(drain) region 951 and second/third doping(source) region ~~951~~ and 952 are disposed in between and on outer sides of the first gates 931 and second gate 932, and coupled to a ~~pad and ground~~ second node 956 and first node 955, respectively. More specifically, the first node 955 is ground while the second node 956 is a pad. The STI 941~944 has portions under the first gates 931

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and second gate 932 and near each end of the first gates 931
and second gate 932 protruding into both the first
doping(drain) region 951 and second/third doping(source)
region ~~951~~ and 952. Each of the first gates 931 and second
5 gate 932 includes a conducting layer 981 made of
polysilicon, an oxide layer 982 made of silicon oxide under
the conducting layer 981 and spacers 983 made of silicon
oxide adjacent to the conducting layer 981 and oxide layer
982.

10 The layout method of the fifth embodiment, increases
the AA' region resistances and decreases parasitic BJT
turning on efficiency, making it possible for ESD current to
go through the BB' region under MM ESD zapping. Thus, the
MM ESD current bypasses bigger areas and has a higher MM ESD
15 level than the device structures of prior arts. Conversely,
the HBM ESD level will not decrease as STI is inserted
between the gate and drain contact or below the gate at the
AA' region.

Eighth Embodiment

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FIG. 12A and 12B are top and sectional views along a line AA' of an ESD protection device according to an eighth embodiment of the invention. For the sake of clarity, the same elements in FIG. 12A and 12B, and 5A and 5B refer to the same symbols. The ESD protection device includes a P silicon substrate 51, STI 52, a P guard ring 50 enclosing the STI 52, first gates 531 and second gate 532, N type first doping(drain) region 551 and second doping(source) region 551—and 552, and third/fourth doping(ESD implantation) regions 591 and 592. The STI 52 is on the substrate 51 and encloses an active region 56. The first gates 531 and second gate 532 have two ends overlapping the STI 52 to stretch over the active region 56, and are coupled to ground or a pre-driver. The first doping(drain) region 551 and second/fifth doping(source) region 551—and 552 are disposed in between and on outer sides of the first gates 531 and second gate 532, and coupled to a pad—and groundsecond node 556 and first node 555, respectively. More specifically, the first node 555 is ground while the

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second node 556 is a pad. The third doping(ESD
implantation) regions 591 and 592 are N type lightly doped
regions disposed under the first doping(drain) region 551
and second/fifth doping(source) region 551 and 552, and near
5 each end of the first gates 531 and second gate 532. The
doping concentrations of the third doping(ESD implantation)
regions 591 and 592 are lower than those of the first
doping(drain) region 551 and second/fifth doping(source)
region 551 and 552. Each of the first gates 531 and second
10 gate 532 includes a conducting layer 581 made of
polysilicon, an oxide layer 582 made of silicon oxide under
the conducting layer 581 and spacers 583 made of silicon
oxide adjacent to the conducting layer 581 and oxide layer
582.

15 In the eighth embodiment, the junction covered by the
proposed ESD implantation has an increased junction
breakdown voltage, because it has a lighter doping
concentration across the p-n junction. The BB' region
without covering the ESD implantation, however, has the

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original junction breakdown voltage, which is lower than the junction breakdown of the ESD implantation region. During the ESD stress, the junction of the BB' region with the lowest junction breakdown voltage will be broken first to
5 discharge the ESD current. As previously mentioned, the AA' region provides a larger bypass area and path for ESD current and has a high MM ESD level. On the other hand, the HBM ESD level will not decrease as the ESD implanted between the gate and drain contact ~~or below the gate~~ at the AA'
10 region. This can also be applied to the PMOS to improve its ESD robustness.

Ninth Embodiment

FIG. 13A and 13B are top and sectional views along a line AA' of an ESD protection device according to an eighth
15 embodiment of the invention. For the sake of clarity, the same elements in FIG. 13A and 13B, and 5A and 5B refer to the same symbols. The ESD protection device includes a P silicon substrate 51, STI 52, a P type fourth doping region(guard ring) 50 enclosing the STI 52, first gates 531

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and second gate 532, N type first doping(drain) region 551
and second doping(source) region 551 and 552, and N type
first doping region wells 593 and second doping region well
594. The STI 52 is on the substrate 51 and encloses an
5 active region 56. The first gates 531 and second gate 532
have two ends overlapping the STI 52 to stretch over the
active region 56, and are coupled to ground or a pre-driver.
The first doping(drain) region 551 and second doping(source)
region 551 and 552 are disposed in between and on outer
10 sides of the first gates 531 and second gate 532, and
coupled to a pad and ground second node 556 and first node
555, respectively. More specifically, the first node 555 is
ground while the second node 556 is a pad. The N type first
wells 593 and second well 594 are disposed under the first
15 doping(drain) region 551, and near ~~each~~ first and second end
of the first gates 531 and second gate 532. Each of the
first gates 531 and second gate 532 includes a conducting
layer 581 made of polysilicon, an oxide layer 582 made of
silicon oxide under the conducting layer 581 and spacers 583

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made of silicon oxide adjacent to the conducting layer 581 and oxide layer 582.

In the ninth embodiment, the MOSFET at the AA' region has a lighter doping concentration (N well) than that of the original (N+) drain junction. Therefore, the junction covered by the proposed N well has an increased junction breakdown voltage, because it has a lighter doping concentration across the p-n junction. However, the BB' region without inserting N well has the original junction breakdown voltage, which is lower than the junction breakdown of the AA' region with N well inserted. During the ESD stress, the junction the BB' region with the lowest junction breakdown voltage will be broken first to discharge the ESD current. As previously mentioned, the AA' region provides a larger bypass area and path for ESD current and has a higher MM ESD level.

Tenth Embodiment

FIG. 14A and 14B are top and sectional views along a line AA' of an ESD protection device according to an eighth

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embodiment of the invention. For the sake of clarity, the same elements in FIG. 14A and 14B, and 5A and 5B refer to the same symbols. The ESD protection device includes a P silicon substrate 51, STI 52, a P guard ring 50 enclosing the STI 52, first gates 531 and second gate 532, and N type first doping(drain) region 551 and second doping(source) region 551 and 552. The STI 52 is on the substrate 51 and encloses an active region 56. The first gates 531 and second gate 532 have two ends overlapping the STI 52 to stretch over the active region 56, and are coupled to ground or a pre-driver. The first doping(drain) region 551 and second/third doping(source) region 551 and 552 are disposed in between and on outer sides of the first gates 531 and second gate 532, and coupled to a ~~pad and ground~~second node 556 and first node 555, respectively. More specifically, the first node 555 is ground while the second node 556 is a pad. The first gates 531 and second gate 532 are bent at an angle so that their center portions protrude into the first doping(drain) region 551. Thus, the widths of the first

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doping(drain) region 551 near the center portions of the
first gates 531 and second gate 532 are smaller than those
near each end of the first gates 531 and second gate 532.
Each of the first gates 531 and second gate 532 includes a
5 conducting layer 581 made of polysilicon, an oxide layer 582
made of silicon oxide under the conducting layer 581 and
spacers 583 made of silicon oxide adjacent to the conducting
layer 581 and oxide layer 582.

In the tenth embodiment, at the AA' region, the drain
10 contact to the poly edge space (DGS) is larger than the
space at the BB' region, therefore the equivalent base
spacing of the parasitic BJT device at the AA' region can be
increased. With a wider base spacing, the BJT will have a
lower turn-on speed and lower current gain. In this
15 structure, the turn-on efficiency of the parasitic BJT at
the AA' region decreases. ESD current will be discharged
through the parasitic BJT at the BB' region under MM ESD
zapping. Thus, the MM ESD current effectively bypasses
bigger areas and has a higher MM ESD level than the device

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structures of the prior arts. Conversely, the HBM ESD level will not decrease and can also be applied to the PMOS to improve its ESD robustness.

In all the previously described embodiments, the
5 layouts are also suitable for PMOS although NMOS is used as an example. They are also suitable for stacked NMOS or PMOS in mixed voltage I/O circuits.

In conclusion, novel ESD protection device structures are proposed in this invention for application under MM ESD
10 stress in sub-quarter-micron CMOS technology. The ESD discharging current path in the NMOS or PMOS device structure is changed by the proposed new structures, therefore the MM ESD level of the NMOS and PMOS can be significantly improved. In this invention, 6 kinds of new
15 structures protect the lateral BJT at the AA' region from current crowding and to balance the turned on efficiency of the lateral BJT at the BB' region. The MM ESD current bypasses through the lateral BJT at the BB' region instead of the AA' region, and has a larger bypass area than the

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prior structures. The current crowding problem can be solved successfully, and have a higher MM ESD robustness. Moreover, these novel devices will not degrade the HBM ESD level and are widely used in ESD protection circuits.

5 The foregoing description of the preferred embodiments of this invention has been presented for purposes of illustration and description. Obvious modifications or variations are possible in light of the above teaching. The embodiments were chosen and described to provide the best
10 illustration of the principles of this invention and its practical application to thereby enable those skilled in the art to utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated. All such modifications and variations are
15 within the scope of the present invention as determined by the appended claims when interpreted in accordance with the breadth to which they are fairly, legally, and equitably entitled.